CLAIMS

1. (Cancelled).

PN 12. (Original) A multiplier comprising:

first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a variable impedance circuit, wherein

said first terminal of said first transistor receives a first input signal, said second terminal thereof is connected to a first potential via a first load, and said third terminal thereof is connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receives a second input signal, said second terminal thereof is connected. to said first potential via a second load, and said third terminal thereof is connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receives said second input signal, said second terminal thereof is connected to said first potential via said first load, and said third terminal thereof is connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receives said first input signal, said second terminal thereof is connected to said first potential via said second load, and said third terminal thereof is connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receives a third input signal , and said third terminal thereof is connected to a second potential via a first impedance device;

said first terminal of said sixth transistor receives a fourth input signal, and said third terminal thereof is connected to said second potential via a second impedance device, and wherein

said variable impedance circuit includes a first resistive element, a variable impedance device, and a second resistive element connected in series between said third terminal of said fifth transistor and said third terminal of said sixth transistor and wherein

a control voltage is applied to a control terminal of said variable impedance device.

3. (Cancelled).

PN 2A. (Currently Amended) A variable gain differential amplifier comprising:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential via a first load, and a third terminal connected to a second potential via a first impedance device;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential via a second load, and a third terminal connected to said second potential via a second impedance device; and

a variable impedance circuit connected between said third terminal of said first transistor and said third terminal of said second transistor, wherein

said variable impedance circuit includes:

first and second variable impedance devices connected in series between said third terminal of said first transistor and said third terminal of said second transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said second potential, and wherein

a control voltage is applied to a control terminal of said first and second variable impedance devices, and

said junction point between said first variable impedance device and said second variable impedance device has a potential different from said second potential due to a voltage drop caused by a current flowing through said resistive element.

PN

35. (Original) A multiplier comprising:

first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a variable impedance circuit, wherein

said first terminal of said first transistor receives a first input signal, said second terminal thereof is connected to a first potential via a first load, and said third terminal thereof is connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receives a second input signal, said second terminal thereof is connected to said first potential via a second load, and said third terminal thereof is connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receives said second input signal, said second terminal thereof is connected to said first potential via said first load, and said third terminal thereof is connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receives said first input signal, said second terminal thereof is connected to said first potential via said second load, and said third terminal thereof is connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receives a third input signal , and said third terminal thereof is connected to a second potential via a first impedance device;

said first terminal of said sixth transistor receives a fourth input signal, and said third terminal thereof is connected to said second potential via a second impedance device, and wherein

said variable impedance circuit includes:

first and second variable impedance devices connected in series between said third terminal of said fifth transistor and said third terminal of said sixth transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said second potential, and wherein

a control voltage is applied to a control terminal of said first and second variable impedance devices.

PN 46. (Original) A variable impedance circuit comprising:

first, second, third, fourth, and fifth nodes;

first and second variable impedance devices connected between said first node and said second node;

a first resistive element connected between said first node and said third node;

a second resistive element connected between said second node and said fourth node; and

a third resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said fifth node, wherein

said first, second, third, fourth, and fifth nodes are supplied with first , second, third, fourth, and fifth potentials respectively,

said first and second potentials being equal, and wherein

a control voltage is applied to a control terminal of said first and second variable impedance devices.

PN

57. (Original) A high-frequency circuit comprising:

a differential amplifier that receives first and second input signals; and

a multiplier, wherein

said differential amplifier comprises:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential via a first load, and a third terminal connected to a second potential via a first impedance device;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential via a second load; and a third terminal connected to said second potential via a second impedance device; and

a variable impedance circuit connected between said third terminal of said first transistor and said third terminal of said second transistor,

said variable impedance circuit including a first resistive element, a variable impedance device, and a second resistive element connected in series between said third terminal of said first transistor and said third terminal of said second transistor,

a control voltage being applied to a control terminal of said variable impedance device, and wherein

said multiplier comprises:

first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a variable impedance circuit,

said first terminal of said first transistor receiving a third input signal, said second terminal thereof being connected to a first potential via a first load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receiving a fourth input signal, said second terminal thereof being connected to said first potential via a second load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receiving said fourth input signal, said second terminal thereof being connected to said first potential via said first load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receiving said third input signal, said second terminal thereof being connected to said first potential via said second load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receiving a fifth input signal, said third terminal thereof being connected to a second potential via a first impedance device;

said first terminal of said sixth transistor receiving a sixth input signal, said third terminal thereof being connected to said second potential via a second impedance device,

said variable impedance circuit including a first resistive element, a variable impedance device, and a second resistive element connected in series between said third terminal of said fifth transistor and said third terminal of said sixth transistor,

a control voltage being applied to a control terminal of said variable impedance device, and wherein

output signals at said second terminals of said first and second transistors in said differential amplifier are applied to said first terminals of said fifth and sixth transistors in said multiplier as said fifth and sixth input signals, and wherein

a first control voltage is applied to said variable impedance circuit in said differential amplifier, and a second control voltage is applied to said variable impedance circuit in said multiplier.

PN

68. (Original) A high-frequency circuit comprising:

a differential amplifier that receives first and second input signals; and

a multiplier, wherein

said differential amplifier comprises:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential via a first load, and a third terminal connected to a second potential via a first impedance device;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential via a second load, and a third terminal connected to said second potential via a second impedance device; and

a variable impedance circuit connected between said third terminal of said first transistor and said third terminal of said second transistor,

said variable impedance circuit including a first resistive element, a variable impedance device, and a second resistive element connected in series between said third terminal of said first transistor and said third terminal of said second transistor,

a control voltage being applied to a control terminal of said variable impedance device, and wherein

said multiplier comprises:

first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a variable impedance circuit,

said first terminal of said first transistor receiving a third input signal, said second terminal thereof being connected to a first potential via a first load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receiving a fourth input signal, said second terminal thereof being connected to said first potential via a second load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receiving said fourth input signal, said second terminal thereof being connected to said first potential via said first load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receiving said third input signal, said second terminal thereof being connected to said first potential via said second load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receiving a fifth input signal, said third terminal thereof being connected to a second potential via a first impedance device;

said first terminal of said sixth transistor receiving a sixth input signal , said third terminal thereof being connected to said second potential via a second impedance device,

said variable impedance circuit including:

first and second variable impedance devices connected in series between said third terminal of said fifth transistor and said third terminal of said sixth transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said second potential,

a control voltage being applied to a control terminal of said first and second variable impedance devices , and wherein

output signals at said second terminals of said first and second transistors in said differential amplifier are applied to said first terminals of said fifth and sixth transistors in said multiplier as said fifth and sixth input signals, and wherein

a first control voltage is applied to said variable impedance circuit in said differential amplifier, and a second control voltage is applied to said variable impedance circuit in said multiplier.

7 9. (Original) A high-frequency circuit comprising:

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a differential amplifier that receives first and second input signals; and

a multiplier, wherein

said variable gain differential amplifier comprises:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential via a first load, and a third terminal connected to a second potential via a first impedance device;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential via a second load, and a third terminal connected to said second potential via a second impedance device; and

a variable impedance circuit connected between said third terminal of said first transistor and said third terminal of said second transistor,

said variable impedance circuit including:

first and second variable impedance devices connected in series between said third terminal of said first transistor and said third terminal of said second transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said second potential,

a control voltage being applied to a control terminal of said first and second variable impedance devices , and wherein

said multiplier comprises:

first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a variable impedance circuit,

said first terminal of said first transistor receiving a third input signal, said second terminal thereof being connected to a first potential via a first load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receiving a fourth input signal, said second terminal thereof being connected to said first potential via a second load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receiving said fourth input signal, said second terminal thereof being connected to said first potential via said first load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receiving said third input signal, said second terminal thereof being connected to said first potential via said second load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receiving a fifth input signal, said third terminal thereof being connected to a second potential via a first impedance device;

said first terminal of said sixth transistor receiving a sixth input signal, said third terminal thereof being connected to said second potential via a second impedance device,

said variable impedance circuit including a first resistive element, a variable impedance device, and a second resistive element connected in series between said third terminal of said fifth transistor and said third terminal of said sixth transistor,

a control voltage being applied to a control terminal of said variable impedance device, and wherein

output signals at said second terminals of said first and second transistors in said differential amplifier are applied to said first terminals of said fifth and sixth transistors in said multiplier as said fifth and sixth input signals, and wherein

a first control voltage is applied to said variable impedance circuit in said differential amplifier, and a second control voltage is applied to said variable impedance circuit in said multiplier.

8 10. (Original) A high-frequency circuit comprising:

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a differential amplifier that receives first and second input signals; and

a multiplier, wherein

said differential amplifier comprises:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential via a first load, and a third terminal connected to a second potential via a first impedance device;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential via a second load, and a third terminal connected to said second potential via a second impedance device; and

a variable impedance circuit connected between said third, terminal of said first transistor and said third terminal of said second transistor,

said variable impedance circuit including:

first and second variable impedance devices connected in series between said third terminal of said first transistor and said third terminal of said second transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said second potential,

a control voltage being applied to a control terminal of said first and second variable impedance devices , and wherein

said multiplier comprises:

first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a variable impedance circuit,

said first terminal of said first transistor receiving a third input signal, said second terminal thereof being connected to a first potential via a first load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receiving a fourth input signal, said second terminal thereof being connected to said first potential via a second load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receiving said fourth input signal, said second terminal thereof being connected to said first potential via said first load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receiving said third input signal, said second terminal thereof being connected to said first potential via said second load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receiving a fifth input signal, said third terminal thereof being connected to a second potential via a first impedance device;

said first terminal of said sixth transistor receiving a sixth input signal, said third terminal thereof being connected to said second potential via a second impedance device,

said variable impedance circuit including:

first and second variable impedance devices connected in series between said third terminal of said fifth transistor and said third terminal of said sixth transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and said second potential,

a control voltage being applied to a control terminal of said first and second variable impedance devices , and wherein

output signals at said second terminals of said first and second transistors in said differential amplifier are applied to said first terminals of said fifth and sixth transistors in said multiplier as said fifth and sixth input signals, and wherein

a first control voltage is applied to said variable impedance circuit in said differential amplifier, and a second control voltage is applied to said variable impedance circuit in said multiplier.

9 M. (Original) A high-frequency circuit comprising:

a differential amplifier; and

a multiplier, wherein

said differential amplifier comprises:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential via a first load, and a third terminal connected to a second potential via a first impedance device;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential via a second load, and a third terminal connected to said second potential via a second impedance; and

a first variable impedance circuit having an impedance connected to said third terminal of said first transistor and said third terminal of said second transistor and varying depending on a first control voltage, and wherein

said multiplier includes first, second, third, fourth, fifth, and sixth transistors each having a first terminal, a second terminal, and a third terminal; and

a second variable impedance circuit,

said first terminal of said first transistor receiving a third input signal, said second terminal thereof being connected to a first potential via a first load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said second transistor receiving a fourth input signal, said second terminal thereof being connected to said first potential via a second load, said third terminal thereof being connected to said second terminal of said fifth transistor;

said first terminal of said third transistor receiving said fourth input signal, said second terminal thereof being connected to said first potential via said first load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fourth transistor receiving said third input signal, said second terminal thereof being connected to said first potential via said second load, said third terminal thereof being connected to said second terminal of said sixth transistor;

said first terminal of said fifth transistor receiving a fifth input signal, said third terminal thereof being connected to said second potential via a first impedance device;

said first terminal of said sixth transistor receiving a sixth input signal, said third terminal thereof being connected to said second potential via a second impedance device,

said second variable impedance circuit being connected between said third terminal of said fifth transistor and said third terminal of said sixth transistor and having an impedance varying depending on a second control voltage, and wherein

output signals at said second terminals of said first and second transistors in said differential amplifier are applied to said first terminals of said fifth and sixth transistors in said multiplier as said fifth and sixth input signals.

12. (Withdrawn) A high-frequency circuit comprising:

a variable gain differential amplifier that receives first and second input signals in a predetermined frequency range; and

a variable gain multiplier from which first and second output signals having a constant frequency are derived, wherein

gains of said variable differential amplifier and said variable gain multiplier are controlled by a common control voltage.

13. (Withdrawn) A differential distributed amplifier comprising:

a first transmission circuit composed of a plurality of inductive elements receiving a first signal;

a second transmission circuit composed of a plurality of inductive elements receiving a second input signal;

a third transmission circuit composed of a plurality of inductive elements;

a fourth transmission circuit composed of a plurality of inductive elements; and

a plurality of differential amplifiers, wherein

canceled

each of said plurality of differential amplifiers comprises:

a first transistor having a first terminal connected to any of said plurality of inductive elements of said first transmission circuit, a second terminal connected to any of said plurality of inductive elements of said third transmission circuit, and a third terminal;

a second transistor having a first terminal connected to any of said plurality of inductive elements of said second transmission circuit, a second terminal connected to any of said plurality of inductive elements of said fourth transmission circuit, and a third terminal; and

a variable impedance circuit connected between said third. terminal of said first transistor and said third terminal of said second transistor, and wherein

said variable impedance circuit includes:

first and second variable impedance devices connected between said third terminal of said first transistor and said third terminal of said second transistor; and

a resistive element connected between a junction point between said first variable impedance device and said second variable impedance device and a reference voltage, and wherein

a control voltage is applied to a control terminal of said first and second variable impedance devices.

14. (Withdrawn) The differential distributed amplifier according to Claim 13, wherein said resistive element includes a constant current source.

15. (Withdrawn) The differential distributed amplifier according to Claim 13, wherein each of said plurality of differential amplifiers further includes:

cancelled

a first impedance device connected between said third terminal of said first transistor and a reference potential; and

a second impedance device connected between said third terminal of said second transistor and a reference potential.

16. (Withdrawn) The differential distributed amplifier according to Claim 15, wherein said first and second impedance devices include a resistance.

17. (Withdrawn) The differential distributed amplifier according to Claim 15, wherein said first and second impedance devices include a constant current source.

18. (Withdrawn) The differential distributed amplifier according to Claim 15, wherein said resistive element includes a constant current source.

19. (Withdrawn) The differential distributed amplifier according to Claim 13, wherein each of said plurality of differential amplifiers further includes:

a third transistor having a first terminal receiving a bias voltage; and

a fourth transistor having a first terminal receiving a bias voltage,

said first and third transistors being cascode-connected, said second and fourth transistors being cascode-connected,

said second terminal of said first transistor being connected via said third transistor to any of said plurality of inductive elements of said third transmission circuit,

Canceled

said second terminal of said second transistor being connected via said fourth transistor to any of said plurality of inductive elements of said fourth transmission circuit.

canceled